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10/570,290	02/28/2006	Adrianus Josephus Bink	NL031031	5446

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EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/570,290	BINK ET AL.	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2008*.

2a)☒ This action is FINAL. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 12/3/2008. At this point, claims 1 and 8 have been amended and claims 19 and 20 have been added . Thus, claims 1-20 are pending in the instant application.

The instant application having Application No. 10/570,290 has a total of 20 claims pending in the application, there are 2 independent claims and 18 dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 5, 7, 8, 13, 14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Cherabuddi (US 6,725,336).

Regarding Claim 1, Cherabuddi teaches an integrated circuit, comprising:

at least one processing unit (CPU 0 and CPU 1 of Figure 2);

a cache memory (L2 cache 23 of Figure 2) having a plurality of memory modules for caching data (the modules are inherently present within the cache as entries which store data in a 2-way set associative described in Column 3 Line

44), wherein the cache memory comprises a plurality of distinct physical banks (the cache is "partitioned into first and second memory partitions, Column 3 Lines 32-33 and Figure 2, and since the memories are made up of SRAM, and SRAM is divided into banks, the partitions are inherently made up of distinct physical SRAM banks), wherein each physical bank comprises some of the memory modules (each processor may have a dedicated cache, Column 2 Lines 10-12, thus each bank inherently has at least some memory modules to store the dedicated data) and is configured to facilitate serving a read/write request independently of other physical banks to allow concurrent transfers for at least two of the physical banks ("CPU 21a may use cache memory partition 23a as a dedicated 2-way associative cache while CPU 21b simultaneously...uses cache memory partition 21b as a dedicated 2-way associative cache", Column 7 Lines 11-14, thus concurrent transfers for the two banks may be used);

remapping means for performing an unrestricted remapping within said plurality of memory modules (a processor may use "both the first and second cache memory partitions", thus remapping means are inherently present to remap the partition 23b of Figure 2 [used for the second processor in a different mode] to join the partition for the first processor), wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules (a processor may use "both the first and second cache memory partitions", thus physical partition 23b [used for the

second processor in a different mode] is remapped to join the physical partition 23a for the first processor).

Regarding Claim 2, Cherabuddi teaches the integrated circuit according to Claim 1, wherein said cache memory is a set-associative cache (Column 2 Lines 1-2).

Regarding Claim 4, Cherabuddi teaches the integrated circuit according to Claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping, wherein the reduction mapping performs the remapping using less output symbols than input symbols (the remapping is done by setting two input signals, C44 and C45, Column 7 Lines 22-29, thus remapping the cache using two input signals and no output signals).

Regarding Claim 5, Cherabuddi teaches all limitations of Claim 1, further comprising:

a Tag RAM unit associated to said cache for identifying which data is cached in said cache memory (tag arrays 61-62 and 63-64 of Figure 4, described in Column 5 Lines 15-19);

wherein said remapping means is arranged in series with said Tag RAM unit (the remapping circuitry is done in the cache access circuitry 22 of Figure 4, which is clearly in series with the Tag RAM unit shown on Figure 4).

Regarding Claim 7, Cherabuddi teaches all limitations of Claim 5, further comprising a look up table for marking faulty memory modules (Column 9 Lines 9-11, the SC bit of each cache entry acts as a look up table for each faulty module).

Regarding Claim 8, Cherabuddi teaches a method of cache remapping in an integrated circuit having at least one processing unit (CPU 0 and CPU 1 of Figure 2); a main memory for storing data (main memory 12 of Figure 1); and a cache memory (L2 cache 23 of Figure 2) having a plurality of memory modules for caching data (the modules are inherently present within the cache as entries which store data in a 2-way set associative described in Column 3 Line 44), the method comprising:

performing an unrestricted remapping within said plurality of modules (a processor may use "both the first and second cache memory partitions", thus remapping is performed to remap the partition 23b of Figure 2 [used for the second processor in a different mode] to join the partition for the first processor), wherein the memory modules are distributed among a plurality of distinct physical banks within the cache memory (the cache is "partitioned into first and second memory partitions, Column 3 Lines 32-33 and Figure 2, and since the memories are made up of SRAM, and SRAM is divided into banks, the partitions are inherently made up of distinct physical SRAM banks), and each physical bank is configured to facilitate serving a read/write request independently of the other physical banks to allow concurrent transfers for at least two of the physical banks banks ("CPU 21a may use cache memory partition 23a as a dedicated 2-way associative cache while CPU 21b simultaneously...uses cache memory partition 21b as a dedicated 2-way associative cache", Column 7 Lines 11-14, thus concurrent transfers for the two banks may be used), wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical

bank of memory modules (a processor may use "both the first and second cache memory partitions", thus physical partition 23b [used for the second processor in a different mode] is remapped to join the physical partition 23a for the first processor).

Regarding Claim 13, Cherabuddi teaches the integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules (since the 2-way set associative caches combine to form a 4-way set associative cache, Column 7 Line 65 to Column 8 Line 1, the remapped memory modules are inherently mapped to a new way).

Regarding Claim 14, Cherabuddi teaches all limitations of Claim 8, wherein the unrestricted remapping is performed on the basis of a reduction mapping using less output symbols than input symbols (the remapping is done by setting two input signals, C44 and C45, Column 7 Lines 22-29, thus remapping the cache using two input signals and no output signals).

Regarding Claim 17, Cherabuddi teaches all limitations of Claim 8, wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules (since the 2-way set associative caches combine to form a 4-way set associative cache, Column 7 Line 65 to Column 8 Line 1, the remapped memory modules are inherently mapped to a new way).

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim rejected under 35 U.S.C. 103(a) as being unpatentable over .

Claim 3, 9-11, and 18 are rejected under U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Asher (US 6,671,822).

Regarding Claim 3, Cherabuddi teaches all limitations of Claim 1 as described above. However, Cherabuddi does not teach a programmable permutation means for remapping. Asher teaches remapping means adapted to perform the remapping on the basis of a programmable permutation function (see bus 18 in Figure 2, which uses a multiplexer to permute way 0 to another given way; it is the multiplexer select bits that enable this permutation mapping to be programmed). It would have been obvious to a person of ordinary skill in the art to which the subject matter pertains at the time the invention was made to have used programmable permutation functions instead of a reduction mapping, since programmable permutation functions allow for greater flexibility in choosing which line to remap to (Column 6 Lines 21-22 in Asher).

Regarding Claim 9, Cherabuddi teaches all limitations of Claim 1 as described above. However, Cherabuddi does not teach evenly distributing faulty memory modules over banks. Asher teaches “remapping defective portions of ways in a set associative

cache to a surrogate portion of another way in the cache" (Column 1 Lines 12-14) thus distributing faulty memory modules over the banks.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the fault remapping of Asher in the remapping means of Cherabuddi, because this "allows for a larger percentage of die to be repaired, with larger usable cache remaining", (Column 1 Lines 23-24).

Regarding Claim 10, Cherabuddi teaches all limitations of Claim 1 as described above. However, Cherabuddi does not teach remapping at a block/line granularity. Asher teaches "remapping defective portions of ways in a set associative cache to a surrogate portion of another way in the cache" (Column 1 Lines 12-14) thus remapping on a line level.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the fault remapping of Asher in the remapping means of Cherabuddi, because this "allows for a larger percentage of die to be repaired, with larger usable cache remaining", (Column 1 Lines 23-24).

Regarding Claim 11, Cherabuddi teaches the integrated circuit according to Claim 1 as described above, wherein the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way within the second physical bank of memory modules (since the 2-way set associative caches combine to form a 4-way set associative cache,

Column 7 Line 65 to Column 8 Line 1, the remapped memory modules are inherently mapped to a new way).

However, Cherabuddi does not teach remapping to a different index. Asher teaches "remapping defective portions of ways in a set associative cache to a surrogate portion of another way in the cache" (Column 1 Lines 12-14) thus changing the index within memory modules.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the fault remapping of Asher in the remapping means of Cherabuddi, because this "allows for a larger percentage of die to be repaired, with larger usable cache remaining", (Column 1 Lines 23-24).

Regarding Claim 18, Cherabuddi teaches the integrated circuit according to Claim 8 as described above, wherein the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way within the second physical bank of memory modules (since the 2-way set associative caches combine to form a 4-way set associative cache, Column 7 Line 65 to Column 8 Line 1, the remapped memory modules are inherently mapped to a new way).

However, Cherabuddi does not teach remapping to a different index. Asher teaches "remapping defective portions of ways in a set associative cache to a surrogate portion of another way in the cache" (Column 1 Lines 12-14) thus changing the index within memory modules.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the fault remapping of Asher in the remapping means of Cherabuddi, because this "allows for a larger percentage of die to be repaired, with larger usable cache remaining", (Column 1 Lines 23-24).

Claim 6 is rejected under U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Kramer (US 4,868,869).

Regarding Claim 6, Cherabuddi teaches all limitations of Claim 1 as been discussed above. However, Cherabuddi does not teach a Tag RAM in parallel with said remapping means. Kramer teaches several lookup tables and additional circuitry (which is what a Tag RAM unit and a remapping unit with Map RAM are) connected in parallel (see Figure 9 in Kramer).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains to have placed the Tag RAM and remapping means of Cherabuddi in parallel as taught by Kramer. As motivation, connecting circuitry in parallel generally leads to a faster circuit. Thus, by putting the units in parallel, additional benefits are obtained.

Claim 12 is rejected under U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Supnik (US 5,070,502).

Regarding Claim 12, Cherabuddi teaches all limitations of Claim 1 as discussed above. However, Cherabuddi does not teach wherein said cache memory comprises a plurality of dynamic random access memory modules. Supnik teaches using a plurality of DRAM modules in a cache (Column 5 Lines 44-54).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used DRAM as banks in the cache memory of Cherabuddi because DRAM are less expensive than other types of memory. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 16, Cherabuddi teaches all limitations of Claim 8 as discussed above. However, Cherabuddi does not teach wherein said cache memory comprises a plurality of dynamic random access memory modules. Supnik teaches using a plurality of DRAM modules in a cache (Column 5 Lines 44-54).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used DRAM as banks in the cache memory of Cherabuddi because DRAM are less expensive than other types of memory. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 19, Cherabuddi teaches all limitations of Claim 1 as discussed above. However, Cherabuddi does not teach wherein said cache memory comprises a plurality of dynamic random access memory modules. Supnik teaches using a plurality of DRAM modules for each separate bank in a cache (Column 5 Lines 44-54).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used DRAM as banks in the cache memory of Cherabuddi because DRAM are less expensive than other types of memory. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 20, Cherabuddi teaches all limitations of Claim 8 as discussed above. However, Cherabuddi does not teach wherein said cache memory comprises a plurality of dynamic random access memory modules. Supnik teaches using a plurality of DRAM modules for each separate bank in a cache (Column 5 Lines 44-54).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used DRAM as banks in the cache memory of Cherabuddi because DRAM are less expensive than other types of memory. Thus, by combining the devices, additional benefits are obtained.

Claim 15 is rejected under U.S.C. 103(a) as being unpatentable over Cherabuddi in view of Emma (US 5,584,002).

Cherabuddi teaches all limitations of Claim 8 as described above. However, Cherabuddi does not teach marking faulty memory modules in a lookup table. Emma teaches marking a look up table for marking faulty memory modules (Column 9 Lines 9-11, the SC bit of each cache entry acts as a look up table for each faulty module).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have marked faulty modules in a lookup table to ensure that the CPU knows which memory modules are defective and does not attempt to use them. Thus, by combining the devices, the additional benefit of keeping the CPU from using a defective memory module (which may result in corrupted data) is obtained.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claims 1 and 8 that Emma does not teach the ability to concurrently serve read/write requests has been considered and is persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of a newly found prior art reference.

Applicant's argument with respect to claims 1 and 8 that Emma teaches merely logical designations instead of physical designations has been considered but is moot in view of the new grounds of rejection.

Applicant's arguments regarding the dependent claims 11, 13, 17, and 18 have been considered but are moot in view of the new grounds of rejection.

CLOSING COMMENTS

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-20 have received a second action on the merits and are subject of a second action final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

February 25, 2009

/Stephen Elmore/
Primary Examiner, Art Unit 2185